Pipelined Carry-Lookahead Generation for a Fast Incrementer

Abstract of Disclosure

An incrementer pipelines the generation of carry lookahead signals. Count registers hold a current count of the incrementer. The current count is fed back as inputs to sum logic, which generates sum bits that are latched into the count registers as a next count. All-ones detect logic detects when all lesser-significance bits in the current count are ones. When all lesser bits are ones, the sum logic toggles the count bit to generate the sum bit for that bit position. Pre-carry logic generates pre-carry lookahead signals from the sum bits. The pre-carry lookahead signals are latched into pipelined carry registers. The pipelined carry registers drive pipelined carry lookahead signals to the all-ones detect logic. Thus carry lookahead signals are generated from a prior sum but used in a next clock cycle to generate then next sum.

Figures